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09/832,867	04/12/2001	Shunpei Yamazaki	740756-2294	1394
31780	7590	02/28/2006	EXAMINER	
ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			LEWIS, MONICA	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/832,867

Applicant(s)

YAMAZAKI ET AL.

Examiner

Monica Lewis

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– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14,25-38 and 51-64 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 51-64 is/are allowed.
- 6) ☒ Claim(s) 1,2,5,6,9,10,13,14,25,26,29,30,33,34,37 and 38 is/are rejected.
- 7) ☒ Claim(s) 3,4,7,8,11,12,27,28,31,32,35 and 36 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 April 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/05;12/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is in response to the request for continued examination filed November 28, 2005.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/28/05 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1-14, 25-38 and 51-64 have been considered but are moot in view of the new ground(s) of rejection.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following must be shown or the feature(s) canceled from the claim(s): a) a driver circuit having a n-channel TFT over a substrate (See Claim 2). No new matter should be entered.

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Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

6. The information disclosure statement filed 12/5/05 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered. The Ekisho reference does not have an abstract or etc. in English.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413).

In regards to claim 1, Ohtani et al. ("Ohtani") discloses the following:

a) a pixel portion having a n-channel TFT and a light emitting element over a substrate (101) (For Example: See Figure 1A);

b) a channel forming region (104) (For Example: See Figure 1A);

c) an n-type impurity region (108) adjacent to the channel forming region (For Example: See Figure 1A);

d) an n-type impurity region (109) adjacent to the n-type impurity region (For Example: See Figure 1A);

e) a gate insulating layer (103) provided over the active layer (For Example: See Figure 1A);

f) a gate electrode (105) provided over the gate insulating layer (For Example: See Figure 1A);

g) a first conductive film (105a) provided over the gate insulating layer (For Example: See Figure 2E);

h) a second conductive film (105b) provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 1A and Figure 2E); and

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i) a protecting film (107) in contact with the gate insulating layer and the second conductive film (For Example: See Figure 1A).

In regards to claim 1, Ohtani fails to disclose the following:

a) a n-type impurity region adjacent to the n-type impurity region.

However, Kamiura et al. ("Kamiura") discloses the use of a n-type impurity region (12) adjacent to the n-type impurity region (11) (For Example: See Figure 1F). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of a n-type impurity region adjacent to the n-type impurity region as disclosed in Kamiura because it aids in lowering OFF current (For Example: See Column 3 Lines 20-25).

Additionally, since Ohtani and Kamiura are both from the same field of endeavor, the purpose disclosed by Kamiura would have been recognized in the pertinent art of Ohtani.

In regards to claim 13, Ohtani discloses the following:

a) the light emitting device is one selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (For Example: See Column 22 Lines 50-55).

9. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413) and Lee et al. (U.S. Patent No. 6,225,150).

In regards to claim 2, Yamazaki discloses the following:

a) pixel portion having a n-channel TFT and a light emitting element over a substrate (For Example: See Figure 1A);

b) a channel forming region (For Example: See Figure 1A);

c) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1A);

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d) an n-type impurity region adjacent to the n-type impurity region
(For Example: See Figure 1A);

e) an n-type impurity region adjacent to the n-type impurity region
(For Example: See Figure 1A);

f) a gate insulating layer provided over the active layer (For Example: See Figure 1A);

g) a gate electrode provided over the gate insulating layer (For Example: See Figure 1A); and

h) a first conductive film provided over the gate insulating layer (For Example: See Figure 1A);

i) a second conductive film provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 1A); and

j) a protection film in contact with the gate insulating film and the second conductive film (For Example: See Figure 1).

In regards to claim 2, Ohtani fails to disclose the following:

a) a n-type impurity region adjacent to the n-type impurity region.

However, Kamiura discloses the use of a n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1F). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of a n-type impurity region adjacent to the n-type impurity region as disclosed in Kamiura because it aids in lowering OFF current (For Example: See Column 3 Lines 20-25).

Additionally, since Ohtani and Kamiura are both from the same field of endeavor, the purpose disclosed by Kamiura would have been recognized in the pertinent art of Ohtani.

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b) a driver circuit having a n-channel TFT over a substrate.

However, Lee et al. ("Lee") discloses the use of a driver circuit having a n-channel TFT over a substrate (For Example: See Figure 3J). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of a driver circuit having a n-channel TFT over a substrate as disclosed in Lee because it aids in preventing off current (For Example: See Column 2 Lines 20-39).

Additionally, since Ohtani and Lee are both from the same field of endeavor, the purpose disclosed by Lee would have been recognized in the pertinent art of Ohtani.

In regards to claim 14, Ohtani discloses the following:

a) the light emitting device is one selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (For Example: See Column 22 Lines 50-55).

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413) and *Silicon Processing* by S. Wolf.

In regards to claim 5, Ohtani discloses the following:

a) the second gate electrode comprises aluminum (For Example: See Column 6 Line 1-6).

In regards to claim 5, Ohtani fails to disclose the following:

a) the first conductive film comprises tungsten.

However, Wolf discloses the use of a conductive film that comprises tungsten (For Example: See Page 398). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use

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of tungsten as disclosed in Wolf because it aids in reducing leakage current (For Example: See Page 398).

Additionally, since Ohtani and Wolf are both from the same field of endeavor, the purpose disclosed by Wolf would have been recognized in the pertinent art of Ohtani.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413), Lee et al. (U.S. Patent No. 6,225,150) and *Silicon Processing* by S. Wolf.

In regards to claim 6, Ohtani discloses the following:

a) the second gate electrode comprises aluminum (For Example: See Column 6 Line 1-6).

In regards to claim 6, Ohtani fails to disclose the following:

a) the first conductive film comprises tungsten.

However, Wolf discloses the use of a conductive film that comprises tungsten (For Example: See Page 398). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of tungsten as disclosed in Wolf because it aids in reducing leakage current (For Example: See Page 398).

Additionally, since Ohtani and Wolf are both from the same field of endeavor, the purpose disclosed by Wolf would have been recognized in the pertinent art of Ohtani.

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12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413) and *Microchip Fabrication* by Peter Van Zant.

In regards to claim 9, Ohtani discloses the following:

a) the gate electrode is covered by an insulating film (111) (For Example: See Figure 1A).

In regards to claim 9, Ohtani fails to disclose the following:

a) the insulating film comprises at least one of a silicon nitride film and a silicon oxynitride film.

However, Van Zant discloses the use of silicon nitride (For Example: See Page 391). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of silicon nitride as disclosed in Van Zant because it aids in providing better protection (For Example: See Page 391).

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413), Lee et al. (U.S. Patent No. 6,225,150) and *Microchip Fabrication* by Peter Van Zant.

In regards to claim 10, Ohtani discloses the following:

a) the gate electrode is covered by an insulating film (For Example: See Figure 1A).

In regards to claim 10, Ohtani fails to disclose the following:

a) the insulating film comprises at least one of a silicon nitride film and a silicon oxynitride film.

However, Van Zant discloses the use of silicon nitride (For Example: See Page 391). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of silicon nitride as disclosed in Van Zant because it aids in providing better protection (For Example: See Page 391).

14. Claims 25 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413) and Sukegawa (Japanese Patent No. JP405257137A).

In regards to claim 25, Ohtani discloses the following:

- a) a pixel portion having a n-channel TFT and a light emitting element over a substrate (For Example: See Figure 1A);
- b) a channel forming region (For Example: See Figure 1A);
- c) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1A);
- d) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1A);
- e) a gate insulating layer provided over the active layer (For Example: See Figure 1A);
- f) a gate electrode provided over the gate insulating layer (For Example: See Figure 1A);
- g) a first conductive film provided over the gate insulating layer (For Example: See Figure 2E); and
- h) a second conductive film provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 1A and Figure 2E).

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In regards to claim 25, Ohtani fails to disclose the following:

- a) a n-type impurity region adjacent to the n-type impurity region.

However, Kamiura discloses the use of a n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1F). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of a n-type impurity region adjacent to the n-type impurity region as disclosed in Kamiura because it aids in lowering off current (For Example: See Column 3 Lines 20-25).

Additionally, since Ohtani and Kamiura are both from the same field of endeavor, the purpose disclosed by Kamiura would have been recognized in the pertinent art of Ohtani.

- b) a coloring layer over the gate electrode.

However, Sukegawa discloses the use of a coloring layer (9) over a gate electrode (2) (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of a coloring layer over the gate electrode as disclosed in Sukegawa because it aids in providing color at a low cost (For Example: See Abstract).

Additionally, since Ohtani and Sukegawa are both from the same field of endeavor, the purpose disclosed by Sukegawa would have been recognized in the pertinent art of Ohtani.

In regards to claim 37, Ohtani discloses the following:

- a) the light emitting device is one selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (For Example: See Column 22 Lines 50-55).

15. Claim 26 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413), Lee et al. (U.S. Patent No. 6,225,150) and Sukegawa (Japanese Patent No. JP405257137A).

In regards to claim 26, Yamazaki discloses the following:

a) pixel portion having a n-channel TFT and a light emitting element over a substrate (For Example: See Figure 1A);

b) a channel forming region (For Example: See Figure 1A);

c) an n-type impurity region adjacent to the channel forming region (For Example: See Figure 1A);

d) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1A);

e) an n-type impurity region adjacent to the n-type impurity region (For Example: See Figure 1A);

f) a gate insulating layer provided over the active layer (For Example: See Figure 1A);

g) a gate electrode provided over the gate insulating layer (For Example: See Figure 1A); and

h) a first conductive film provided over the gate insulating layer (For Example: See Figure 1A); and

i) a second conductive film provided over the first conductive film, wherein the first conductive film overlaps the channel forming region and the n type impurity region with the gate insulating layer interposed therebetween, and wherein the second conductive film overlaps the channel forming region with the gate insulating layer and the first conductive film interposed between (For Example: See Figure 1A).

In regards to claim 26, Ohtani fails to disclose the following:

a) a n-type impurity region adjacent to the n-type impurity region.

However, Kamiura discloses the use of a n-type impurity region adjacent to the

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n-type impurity region (For Example: See Figure 1F). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of a n-type impurity region adjacent to the n-type impurity region as disclosed in Kamiura because it aids in lowering OFF current (For Example: See Column 3 Lines 20-25).

Additionally, since Ohtani and Kamiura are both from the same field of endeavor, the purpose disclosed by Kamiura would have been recognized in the pertinent art of Ohtani.

b) a driver circuit having a n-channel TFT over a substrate.

However, Lee discloses the use of a driver circuit having a n-channel TFT over a substrate (For Example: See Figure 3J). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of a driver circuit having a n-channel TFT over a substrate as disclosed in Lee because it aids in preventing off current (For Example: See Column 2 Lines 20-39).

Additionally, since Ohtani and Lee are both from the same field of endeavor, the purpose disclosed by Lee would have been recognized in the pertinent art of Ohtani.

c) a coloring layer over the gate electrode.

However, Sukegawa discloses the use of a coloring layer (9) over a gate electrode (2) (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of a coloring layer over the gate electrode as disclosed in Sukegawa because it aids in providing color at a low cost (For Example: See Abstract).

Additionally, since Ohtani and Sukegawa are both from the same field of endeavor, the purpose disclosed by Sukegawa would have been recognized in the pertinent art of Ohtani.

In regards to claim 38, Ohtani discloses the following:

a) the light emitting device is one selected from the group consisting of an EL display, a video camera, a digital camera, a portable computer, a personal computer, a portable telephone, and a car audio stereo (For Example: See Column 22 Lines 50-55).

16. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413), Sukegawa (Japanese Patent No. JP405257137A) and *Silicon Processing* by S. Wolf.

In regards to claim 29, Ohtani discloses the following:

a) the second gate electrode comprises aluminum (For Example: See Column 6 Line 1-6).

In regards to claim 29, Ohtani fails to disclose the following:

a) the first conductive film comprises tungsten.

However, Wolf discloses the use of a conductive film that comprises tungsten (For Example: See Page 398). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of tungsten as disclosed in Wolf because it aids in reducing leakage current (For Example: See Page 398).

Additionally, since Ohtani and Wolf are both from the same field of endeavor, the purpose disclosed by Wolf would have been recognized in the pertinent art of Ohtani.

17. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413), Lee et al. (U.S. Patent No. 6,225,150) and Sukegawa (Japanese Patent No. JP405257137A) and *Silicon Processing* by S. Wolf.

In regards to claim 30, Ohtani discloses the following:

a) the second gate electrode comprises aluminum (For Example: See Column 6 Line 1-6).

In regards to claim 30, Ohtani fails to disclose the following:

a) the first conductive film comprises tungsten.

However, Wolf discloses the use of a conductive film that comprises tungsten (For Example: See Page 398). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of tungsten as disclosed in Wolf because it aids in reducing leakage current (For Example: See Page 398).

Additionally, since Ohtani and Wolf are both from the same field of endeavor, the purpose disclosed by Wolf would have been recognized in the pertinent art of Ohtani.

18. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413), Sukegawa (Japanese Patent No. JP405257137A) and *Microchip Fabrication* by Peter Van Zant.

In regards to claim 33, Ohtani discloses the following:

a) the gate electrode is covered by an insulating film (For Example: See Figure 1A).

In regards to claim 33, Ohtani fails to disclose the following:

a) the insulating film comprises at least one of a silicon nitride film and a silicon oxynitride film.

However, Van Zant discloses the use of silicon nitride (For Example: See Page 391). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of silicon nitride as disclosed in Van Zant because it aids in providing better protection (For Example: See Page 391).

19. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani et al. (U.S. Patent No. 6,259,138) in view of Kamiura et al. (U.S. Patent No. 6,288,413), Lee et al. (U.S. Patent No. 6,225,150), Sukegawa (Japanese Patent No. JP405257137A) and *Microchip Fabrication* by Peter Van Zant.

In regards to claim 34, Ohtani discloses the following:

a) the gate electrode is covered by an insulating film (For Example: See Figure 1A).

In regards to claim 34, Ohtani fails to disclose the following:

a) the insulating film comprises at least one of a silicon nitride film and a silicon oxynitride film.

However, Van Zant discloses the use of silicon nitride (For Example: See Page 391). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ohtani to include the use of silicon nitride as disclosed in Van Zant because it aids in providing better protection (For Example: See Page 391).

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Allowable Subject Matter

20. Claims 3, 4, 7, 8, 11, 12, 27, 28, 31, 32, 35 and 36 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. Claims 51-64 are allowed.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

January 30, 2006

A handwritten signature in black ink, appearing to be 'C. Lewis', is located in the bottom right corner of the page.